Amendment to the Claims

1-4. (Cancelled)

5. (Currently Amended) ~~The~~ A system ~~of claim 25~~ for resequencing received data packets comprising:

a first means for storing each received data packet at an allocated location within said first means;

a Content Address Memory (CAM) having at least one entry comprising an identification field to contain a packet buffer identifier (ID) field to identify an allocated location in said first means whereat a received data packet is placed, a search field to contain a source identifier of a source providing said receive data packet, a priority level for said receive data packet and a sequence number for said receive data packet, wherein recited fields are concatenated;

a plurality of source-priority registers each containing, a packet sequence number (PSN) and a packet buffer identifier (ID) of a data packet previously transmitted from said first means; and

a plurality of valid-bit latches respectively associated to the plurality of source-priority registers to set an active status to indicate that corresponding stored data packet is the next one in sequence, wherein the number of source-priority registers and associated valid-bit latches are equal to the number of sources providing packets multiply by number of priority levels.

6. (Previously Presented) The system of claim 5 wherein each of the plurality of source-priority registers further comprise counting means to count for each sequence of data packets the number of data packets stored within said storing means waiting for being output from at least one egress adapter.

7. (Previously Presented) The system of claims 6 further comprising scheduling means (280) coupled to the CAM and the plurality of source priority registers for selecting one sequence of data packets from which a data packet is to be output from the at least one egress adapter.

8. (Original) The system of claim 7 wherein the scheduling means are coupled to the plurality of valid-bit latches to select one valid-bit latch among the valid-bit latches having their valid bit active.

9-25. (Cancelled)